A Cost-Effective Method for Accurate PCB Impedance Simulation of Any Specific Stack-Ups

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Abstract
This paper analyzes the reasons of inaccurate PCB impedance simulation of the traditional simulator and introduces a novel and cost-effective method for accurate PCB impedance simulation of any specific stack-ups. The new method doesn't need to extract material properties from prototype boards or empirical modified DK from PCB Fabs. The test results show the new method & tool have better precision simulation ability with deviation less than 2.5%, compared with traditional simulation tool. It can meet the requirement of less than 5% tolerance impedance to match the high speed & high frequency PCB design, and consequently leads to a more cost-saving and time-saving method to rapidly occupy the market.

Introduction
Impedance control plays an important role for both PCB designer and PCB Fabs. The accuracy of impedance simulation is the key factor to meet the spec and control cost. Nevertheless, through a large quantity of research papers [1][2] and product data, which I obtained from some PCB Fabs, it is indicated that there is a big deviation on PCB impedance simulation, often off by >5%, and the most off range:5%~15%, even more than 15%.

Reasons of the inaccurate PCB impedance Simulation

1. Non-uniform DK distribution of FR4 mixed dielectric:
   PCB FR4 base material is a mixed dielectric with glass [DK: 4~6.5] and epoxy resin [DK: 2~3.5]. The DK measured from Prepreg or Core is the average DK of the mix dielectric, See Figure 1.

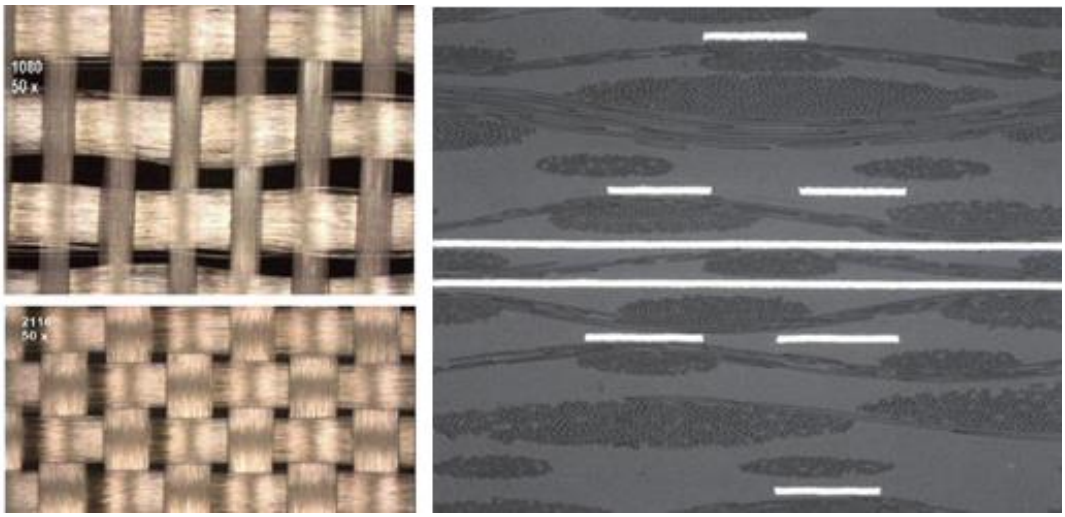


Figure 1: FR4 glass-resin mix dielectric

2. Electromagnetic field distribution is also Non-uniform:
   We used FDTD method to image the impedance model Electromagnetic field distribution. From Figure 2 we can see the strong electromagnetic field is around the trace, but the area around trace is covered by the pure resin with lower DK value than the measured average DK (In rare cases the trace will touch the glass fabric without resin fully covered, and this case is abnormal).

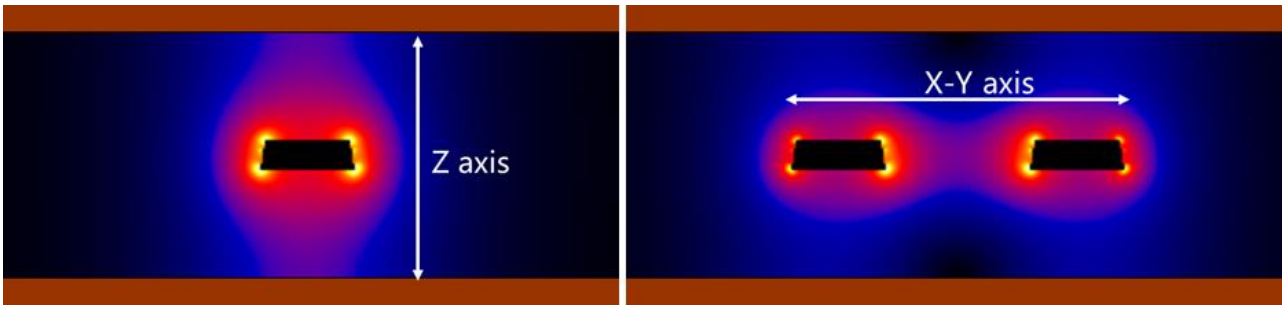


Figure 2: Stripline Model Electromagnetic field distribution

And we can also see the Single-end stripline is sensitive to the DK on Z axis (on/below the trace), that means the Single-end model will have more variation due to Fiber Wave Effect [3]. The Differential stripline is sensitive to DK on X-Y axis (around/filled the two traces). So, the resin-filled layer will be a non-negligible and important factor for PCB Impedance simulation. And the value of resin DK will dominate the impedance especially on the differential stripline model, See Figure 3.

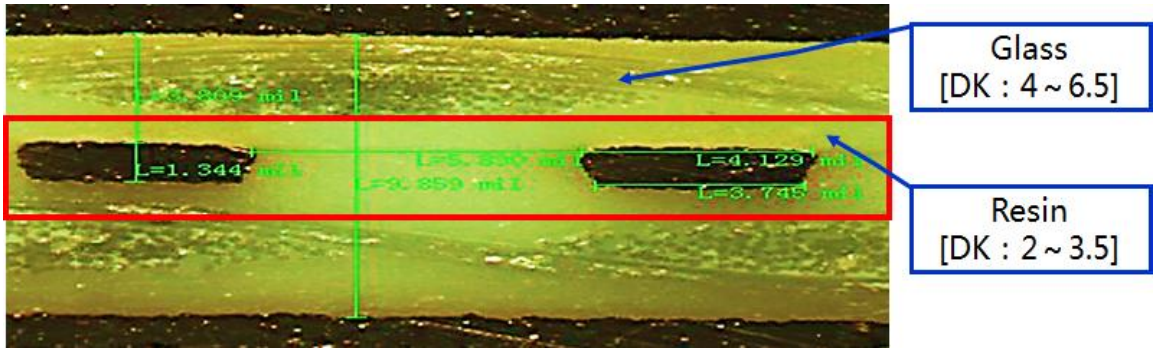
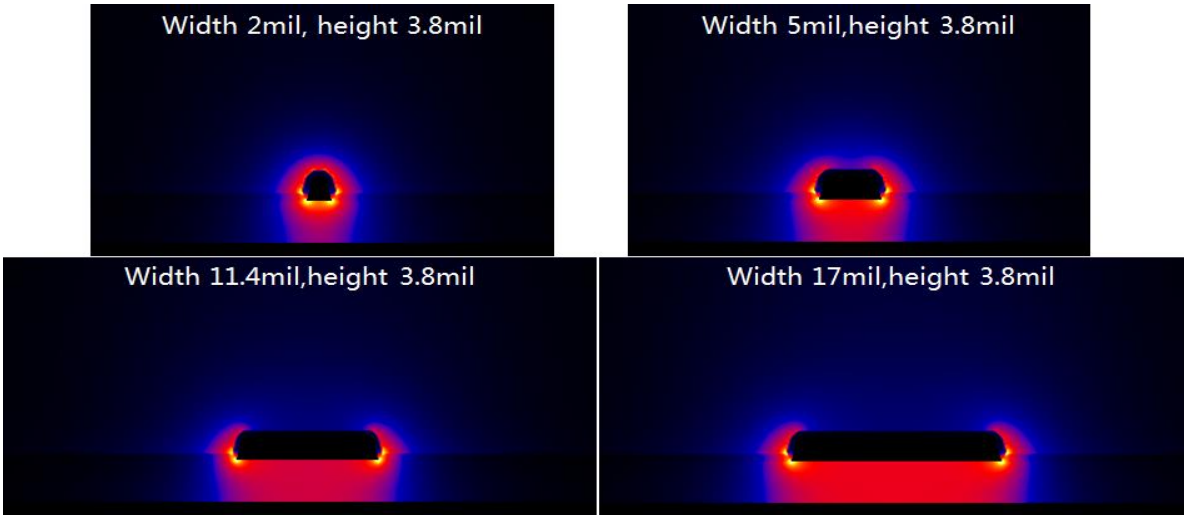


Figure 3: Resin-filled layer on differential stripline



The third important finding is that the impedance model Electromagnetic field distribution will be effected by the model geometries (trace width=W, trace thickness=T, dielectric height=H etc.). So on a fixed stack-up (DK distribution is fixed) if the trace width is changed, the final effective DK will be different, See Figure 4.

Figure 4: Microstrip Electromagnetic field distribution effected by model geometries

3. The problem of the Traditional impedance filed solver on resin-filled layer:

Polar si8000/si9000 is the most used field solver for impedance simulation. I once made an experiment to compare the impedance model with/without resin-filled layer when I worked at Viasystem GZ 10 years ago.

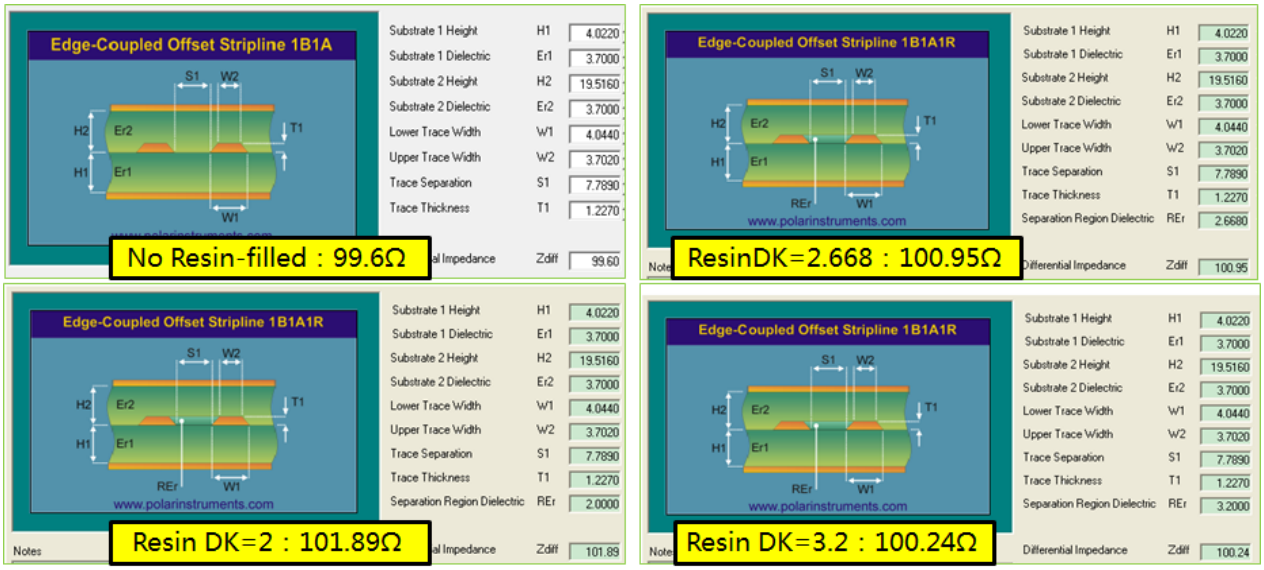


Figure 5: Compare the model with/without resin-filled layer with same geometries

The results show Polar's resin-filled model doesn't have obvious difference from the normal Non-resin-filled model. And there is still a big gap with measured 109 Ohm. Hence, we can summary the root cause in a word: The real effective DK is multivariable, but we use a fixed DK for design simulation.

Empirical DK method

In the past 30 years, most PCB Fabs adopt one of the two methods: (1) Impedance offset; (2) Empirical DK to design the boards. The Empirical DK is the most used method, and it was suggested by Polar AP139 [2]. Polar suggests reducing 10%~15% in datasheet DK. The table on Figure 6 showed some empirical DK we collected from test boards. The difference between datasheet DK and back-calculated DK is not fixed. As a result, it uses the average of the back-calculated DKs as the empirical DK, which means the empirical DK is still a fixed value. So, the problem still exists.

Figure 6: Empirical DK vs. the Datasheet DK

Test boards DK analysis Summary					
Base Material	PP Style	DK Simulation			
		CITS25	SI8000	Datasheet	Difference
Isola-FR408	1080 RC63%	3.08	3.12	3.51	0.39
Isola-FR408	2116 RC53%	3.12	3.13	3.73	0.6
Isola-IS415	1080 RC65%	3.05	3.02	3.52	0.5
Isola-IS415	2116 RC55%	3.06	3.08	3.72	0.64
TUC-TU862	1080 RC67%	3.4	3.43	4.1	0.67
TUC-TU862	2116 RC56%	3.63	3.6	4.3	0.7
TUC-TU862	2116 RC60%	3.8	3.81	4.3	0.49
EMC-EM370D	1080 RC63%	3.24	3.28	3.8	0.52
EMC-EM370D	2116 RC52%	3.47	3.44	4.1	0.66
EMC-EM370D	7629 RC44%	3.66	3.7	4.2	0.5
ITEQ-IT200LK	1080 RC65%	3.14	3.15	3.68	0.53
ITEQ-IT200LK	2116 RC57%	3.14	3.13	3.83	0.7
ITEQ-IT200LK	7628 RC50%	3.31	3.3	3.99	0.69

The Empirical DK method will help on the simple design (10% tolerance; ≤8 layers; ≤10 impedance items). The effect will be significantly reduced in more complicated designs. As tolerance requirements become more stringent, the drawbacks of the empirical DK method become more apparent.

A. 10% tolerance control capability limit

Currently 10% impedance tolerance is the capability limit for the mass production of almost all the PCB Fabs. There is a very interesting question: Why 10% tolerance is the ultimate capability of high-end Fabs and low-end Fabs?

According to our research, the manufacturing process capability [Dielectric uniformity, copper thickness uniformity, line width uniformity] ranges from about 2.5~3.5% with little difference, refer to Figure 11; the design capability [simulation accuracy] ranges from about 6 %~15% (Using empirical DK). This is a good explanation of why industry capabilities can only reach 10% tolerance requirement, because everyone uses the same simulation tool and method.

Figure 7: Dielectric structure stratification of specific stack-up

B. Black-Box---Impedance design rule in transparency

In generally the front-end designer (Customer) only provides a rough reference design using the datasheet DK to the PCB Fabs (Vendor). The PCB fab manages to meet the requirement using private empirical DK. The customer will rely on the PCB Fabs experience to meet the requirement. That means it's hard to assess the risk until the boards manufactured.

C. Cost and Yield Rate

As is known to all, it's very expensive to build the empirical DK database. The yield rate of the empirical DK method is not as good as expected. According to quality report obtained from some big PCB Fabs, the FPY is around 50% ~65%, and even <30% for some NPIs. The industry needs a reasonable and cost-effective method to meet the cost and tighten tolerance requirement.

The cost-effective Solution

From the analysis of Reasons of the inaccurate PCB impedance Simulation, we know the core issue is using Fixed DK for design. So we need to find a systematic approach to define DK distribution of a specific stack-up. And then we need to build the special multilayers impedance model which is compatible with the FR4 dielectric structure. Following this approach, we can improve the capability to 5% only relying on the simulation technique. That will help us to save lots of investment and time.

- **Key Procedure:**
  1. **Specific stack-ups (DK) simulation:**
     - **A.** Dielectric structure stratification:

     Each single Prepreg can be divided into two kinds of layers: resin layer and glass-resin mixed layer

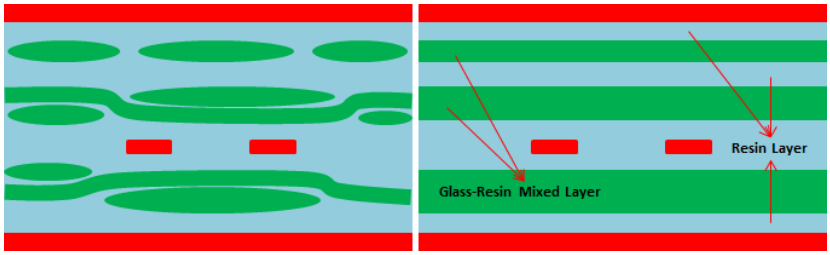


Figure 8: Dielectric structure stratification of specific stack-up

B. Calculating the thickness of each resin layer and glass-resin mixed layer:

C. DK simulation:

Building Model to get the DK of resin layer (DK_Resin) and the DK of glass-resin mixed layer (DK_mix) from the measured DK of raw base material Prepreg/Core (DK_Average)

2. Building a high accurate multilayers impedance model field solver with resin-filled layer:

We used the same model and parameters showed on Figure 5 to validate the accuracy of the new solver. From Figure 7, we can see the new solver cans accurately show the Resin DK effect as Resin DK changed.

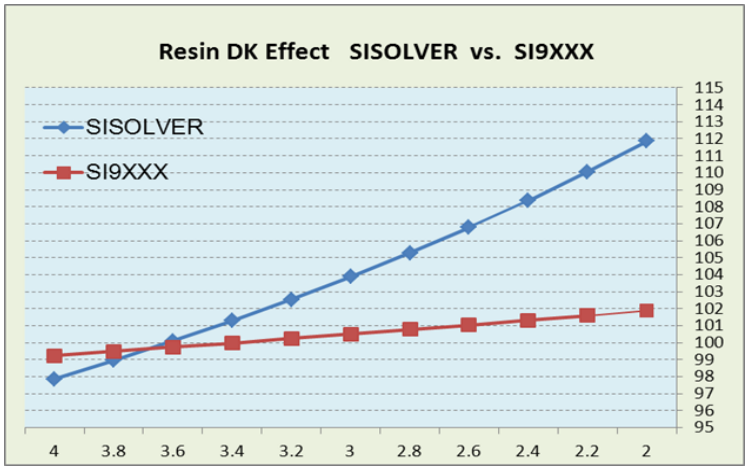


Figure 9: Resin DK effect comparison

Case Study:

We built a 10 layers test board with ISOLA's IS415 base material and designed 4 different impedance models on a coupon. There were 16 test coupons on the board. Will take 1 stripline model (Sig: L5; Ref: L4/L7 with target 110 ohm) as the sample for analysis and collect data from the 48 microsections (3 points/coupon, 16 coupons). The stack-up, test board and impedance coupon illustration are demonstrated on **Figure 10.**

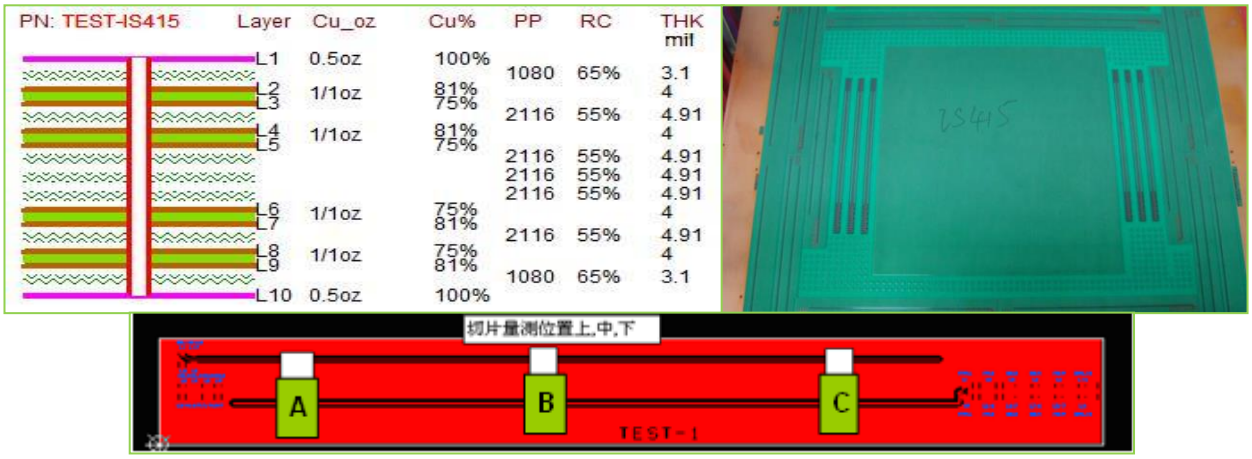


Figure 10: The stack-up, test board and impedance coupon

1. Microsection&Impedance data analysis:

The raw data of the microsection datasheet please refer to the Attachment 1 on the last page. The Cpk of the measured impedance data is very good. As shown in Figure 11, the manufacturing process was in good control with very little variation. Then we will use the average impedance 109 Ohm as the simulation target for further analysis.

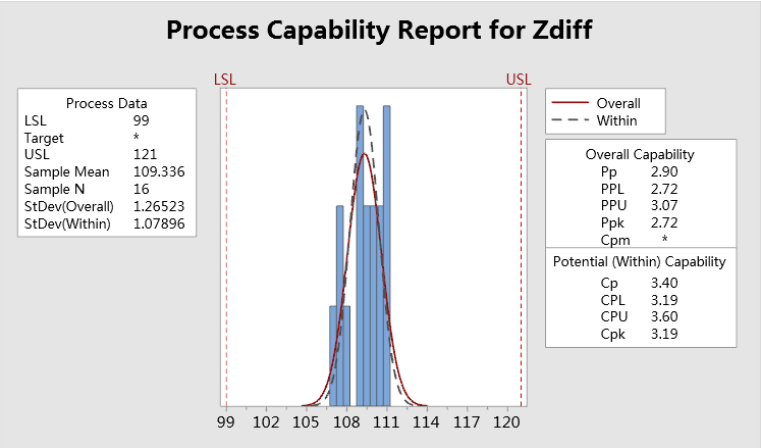


Figure 11: process capability analysis

2. Simulation:

As the measured impedance of No.15 is the most close the average 109 Ohms. We choose No.15 coupon for simulation. And then used FDTD method to image the Electromagnetic field distribution of the microsection, see **Figure 11.**

Coupon No.	Microsection [Sig:L5; Ref:L4/L7] (mil)							Zdiff (Ohm)
	Location	H(H1+H2)	H1	W2	W1	S	T	
15	A	23.451	4.001	3.777	4.033	7.746	1.152	109.044
	B	24.045	4.129	3.585	4.033	7.842	1.248	
	C	23.120	3.937	3.745	4.065	7.778	1.280	
	Average	23.539	4.022	3.702	4.044	7.789	1.227	

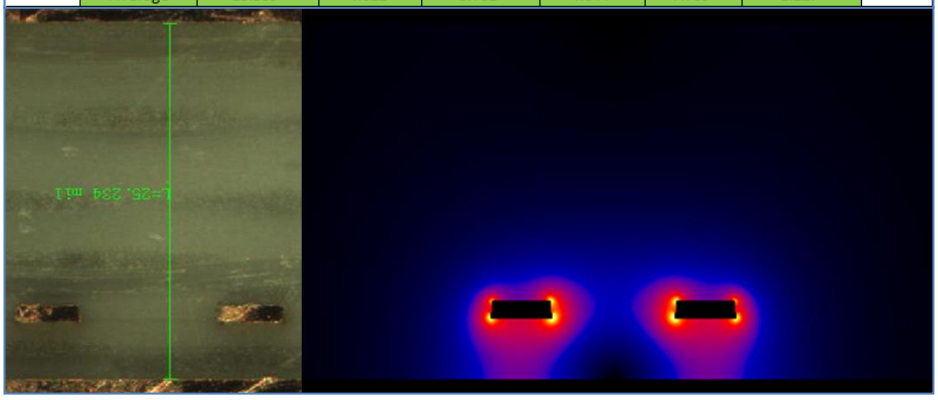


Figure 11: Microsection and Electromagnetic field distribution

- **Building the stack-up with datasheet DK for simulation.** Some calculated key parameters refer to **Figure 12.**
  Space: the finish dielectric thickness after pressed
  M_DK: the Mixed-DK of the dielectric space after pressed
  Bcoat: the buttercoat thickness of the space

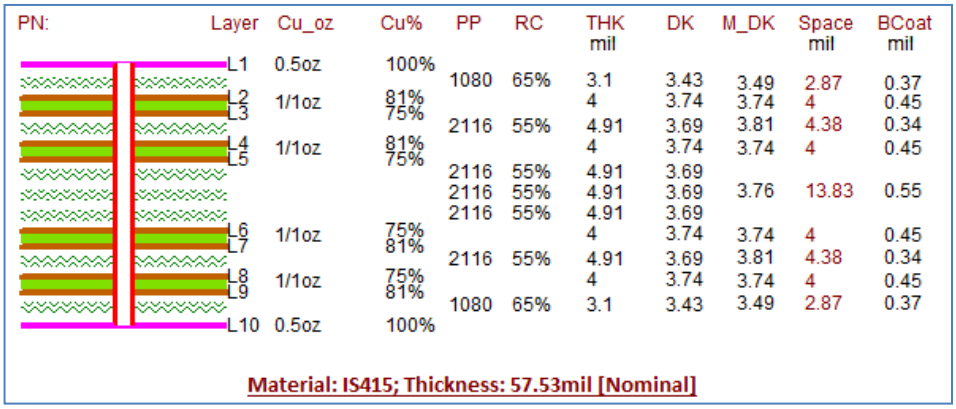


Figure 12: Stack-up & DK simulation

- **Impedance Model simulation**, refer to **Figure 13**

The new field solver auto-links to the stack-up and gets all the parameters including some hidden parameters calculated at the Stack-up simulation step (Buttercoat thickness, DK_Resin, DK_Glass etc.) in order to reduce the complexity of the operation. The calculated impedance is 107 Ohm, closed to the measured 109 Ohm, off by 1.8%. The simulation result of traditional field solver is near 100 Ohm, off by 9%, refer to **Figure 5.**

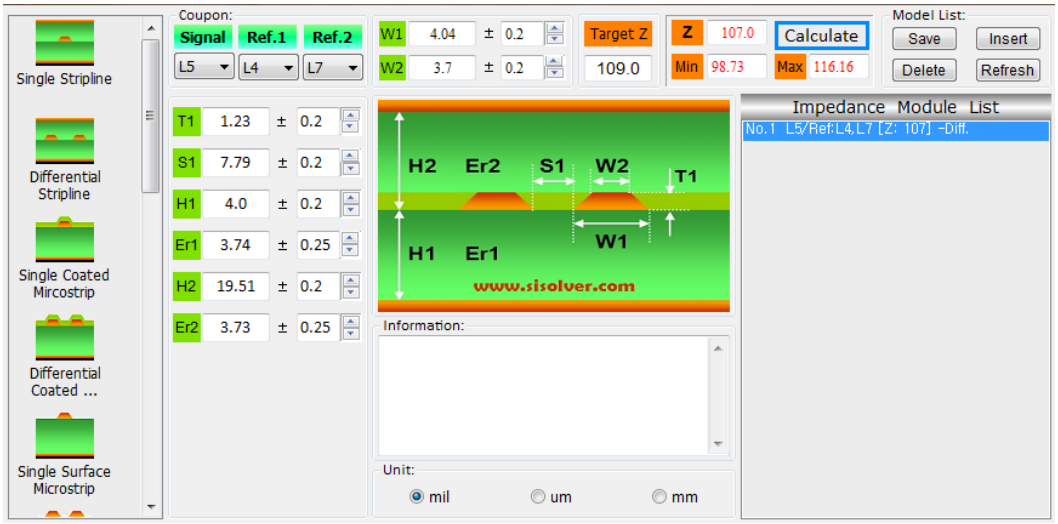


Figure 13: Impedance Model simulation

The Accuracy of the new method

In the past 5 years, we tested over 100 PNs including mass volume and prototype PNs up to 48 Layers, and tested the most mainstream base materials including ISOLA (IS415, I-SPEED), ITEQ (IT180A, IT968, IT988, IT933+), TUC (TU862HF, TU863, TU883, TU933+), PANASONIC (M4, M6, M6N, M7, M7N) etc. The test results are very good, and the deviation is about 2.5%, refer to **Figure 14**. And the test results confirm our analysis discussed in the previous section: the Single-end model has more variation than the Differential model due to the Fiber Wave Effect.

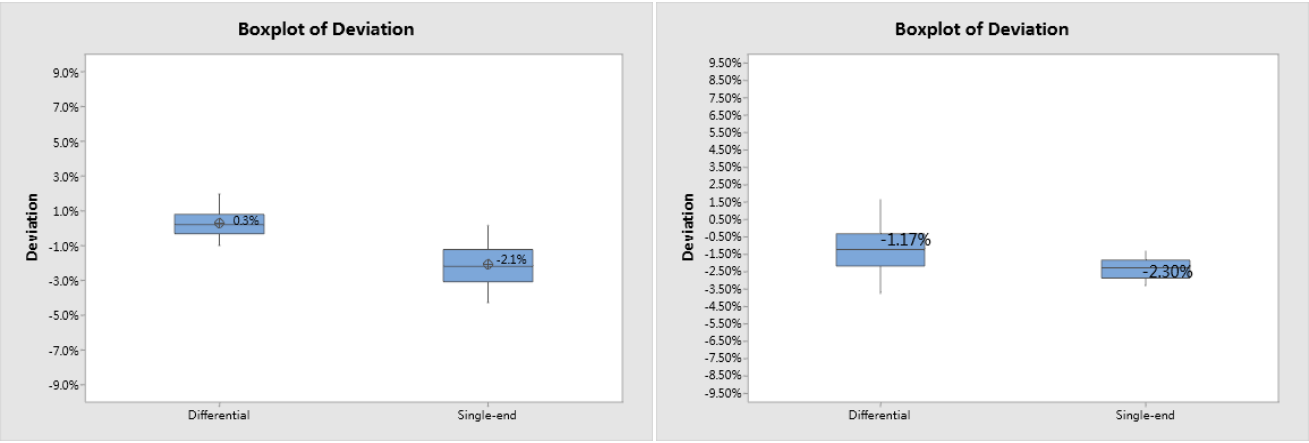


Figure 14: Deviation of simulation

Summary

- DK distribution of FR4 mixed dielectric is not uniform, and Electromagnetic field distribution of impedance model is not uniform too.
- Traditional method uses a fixed DK to design, but the real effective DK is multivariable.
- 10% impedance tolerance is the ultimate limit of the empirical DK method, and it helps only for some simple boards.
- Empirical DK method results in the Black-Box of impedance design process. The non-transparent Black-Box lead to problems on the quality, cost and lead-time.

- The introduced new method using the specific stack-up & DK simulation technique and multilayers dielectric field solver with resin-filled layer can achieve <2.5% tolerance.
- The new method is novel and cost-effective without any empirical data involved. It helps to achieve 5% tolerance spec and save lots of cost and time.

References

[1] Jeff Loyer, Andy Burkhardt, Richard Kunze, Richard Attrill "ACCURATE INSERTION LOSS AND IMPEDANCE MODELING OF PCB TRACES", DesignCon, 2013

[2] "Impedance – measured v calculated in woven glass reinforced laminates", https://www.polarinstruments.com/support/cits/AP139.html

[3] Gerardo Romo L, Chudy Nwachukwu, Reydezel Torres-Torres, Seung-Won Baek, Martin Schauer "Stack-up and routing optimization by understanding micro-scale PCB effects", DesignCon, 2011

Attachment 1

Coupon No.	Microsection [Sig:L5; Ref:L4/L7] (mil)							Zdiff (Ohm)
	Location	H(H1+H2)	H1	W2	W1	S	T	
1	A	24.970	3.937	3.841	4.065	7.746	1.152	109.062
	B	24.904	3.937	3.649	3.905	7.810	1.216	
	C	24.639	3.969	3.777	4.097	7.714	1.248	
	Average	24.838	3.948	3.756	4.022	7.757	1.205	
2	A	25.102	3.873	3.777	4.065	7.778	1.280	110.139
	B	25.234	3.969	3.457	3.745	8.034	1.216	
	C	25.234	3.873	3.681	3.841	8.194	1.184	
	Average	25.190	3.905	3.638	3.884	8.002	1.227	
3	A	24.904	3.873	3.745	3.937	7.906	1.248	108.759
	B	24.315	4.033	3.777	4.097	7.650	1.312	
	C	24.639	3.969	3.777	4.097	7.714	1.248	
	Average	24.619	3.958	3.766	4.044	7.757	1.269	
4	A	24.772	3.905	3.873	4.033	7.746	1.312	109.964
	B	24.771	3.905	3.713	3.937	7.906	1.344	
	C	24.573	3.937	3.617	3.905	7.810	1.248	
	Average	24.705	3.916	3.734	3.958	7.821	1.301	
5	A	25.102	3.905	3.809	3.969	7.842	1.248	108.243
	B	25.366	4.065	3.777	3.937	7.874	1.152	
	C	24.838	3.809	3.841	4.033	7.874	1.472	
	Average	25.102	3.926	3.809	3.980	7.863	1.291	
6	A	23.622	3.905	3.649	3.841	7.066	1.248	109.448
	B	24.639	3.937	3.713	3.937	7.906	1.280	
	C	24.904	3.937	3.457	3.649	8.034	1.152	
	Average	24.388	3.926	3.606	3.809	7.669	1.227	
7	A	23.979	4.065	3.617	3.809	7.970	1.280	110.454
	B	24.507	3.969	3.553	3.873	7.970	1.216	
	C	24.243	3.841	3.361	3.681	8.066	1.248	
	Average	24.243	3.958	3.510	3.788	8.002	1.248	
8	A	25.102	4.065	3.713	4.033	7.874	1.312	110.278
	B	25.554	4.065	3.681	4.001	7.874	1.184	
	C	24.904	3.841	3.649	4.065	7.746	1.312	
	Average	25.187	3.990	3.681	4.033	7.831	1.269	
9	A	25.234	4.033	3.649	3.649	7.906	1.280	110.761
	B	24.705	3.969	3.553	3.681	8.098	1.216	
	C	24.705	3.873	3.617	3.873	7.906	1.344	
	Average	24.881	3.958	3.606	3.734	7.970	1.280	
10	A	24.705	4.001	3.841	4.097	7.778	1.280	109.641
	B	24.772	3.969	3.777	3.905	7.874	1.280	
	C	25.498	3.905	3.873	4.161	7.810	1.280	
	Average	24.992	3.958	3.830	4.054	7.821	1.280	
11	A	23.912	3.745	3.937	4.225	7.81	1.312	110.857
	B	24.809	3.969	3.745	3.969	7.842	1.248	
	C	24.573	3.873	3.681	4.001	7.810	1.344	
	Average	24.431	3.862	3.788	4.065	7.821	1.301	
12	A	25.168	3.841	3.969	4.321	7.522	1.376	107.016
	B	25.366	3.905	3.809	4.097	7.778	1.312	
	C	24.705	3.905	3.841	4.225	7.714	1.344	
	Average	25.080	3.884	3.873	4.214	7.671	1.344	
13	A	24.837	3.841	3.841	4.001	7.810	1.376	107.455
	B	24.837	3.937	3.841	4.161	7.714	1.312	
	C	24.573	3.873	3.873	4.225	7.746	1.440	
	Average	24.749	3.884	3.852	4.129	7.757	1.376	
14	A	24.772	3.841	3.777	4.097	7.682	1.248	107.442
	B	25.036	3.969	3.617	3.873	7.970	1.216	
	C	24.248	4.001	3.649	4.033	7.778	1.152	
	Average	24.685	3.937	3.681	4.001	7.810	1.205	
15	A	23.451	4.001	3.777	4.033	7.746	1.152	109.044
	B	24.045	4.129	3.585	4.033	7.842	1.248	
	C	23.120	3.937	3.745	4.065	7.778	1.280	
	Average	23.539	4.022	3.702	4.044	7.789	1.227	
16	A	24.243	3.905	3.681	3.937	7.908	1.248	110.816
	B	24.509	4.161	3.745	4.003	7.810	1.248	
	C	23.781	3.937	3.745	3.969	7.938	1.216	
	Average	24.178	4.001	3.724	3.970	7.885	1.237	

Table 1: The microsection and measured impedance data

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A Cost-effective Method for Accurate PCB Impedance Simulation of Any Specific Stack-ups

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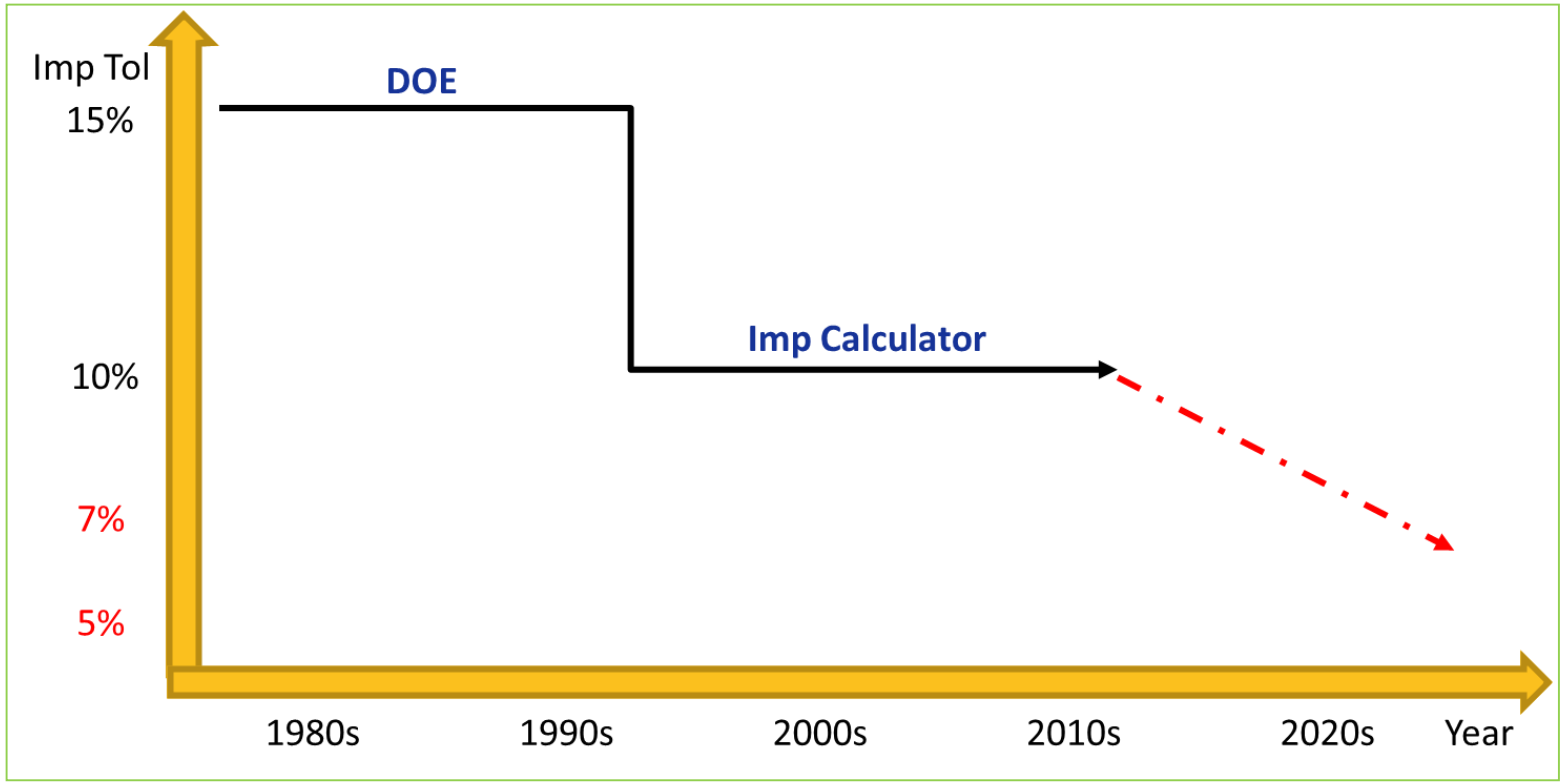
Overview

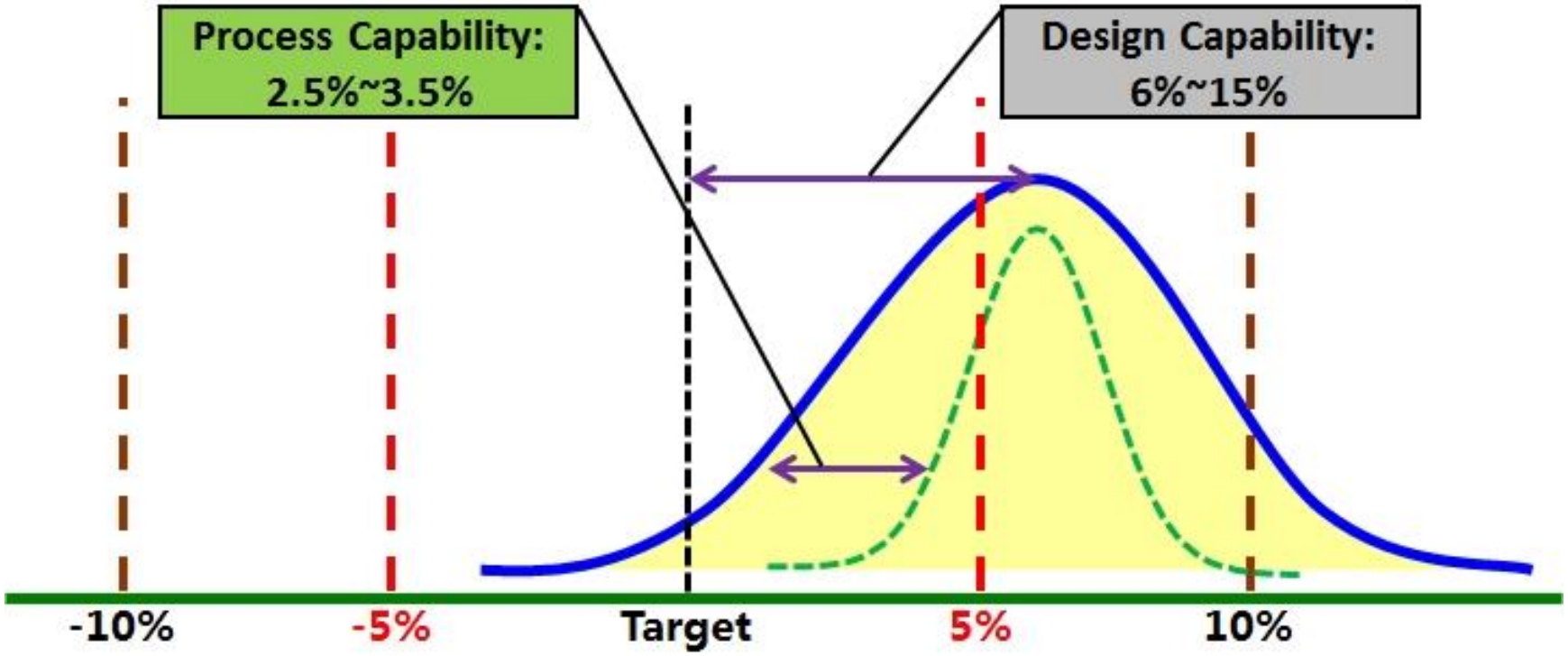
- Background
- Reasons of the inaccurate impedance simulation
- Traditional Empirical Dk method
- Cost-effective new method
  - *Key Procedure*
  - *Case Study*
  - *Accuracy of the new method*
- Summary

Trend of Impedance control:



- **7%, 5% tol. requirements become more stringent, but mainstream capability of indurstry is 10%.**

Capability:



- **Base on the long-term product data collected from Fabs, the manufacturing process capability is good compared to the design simulation capability.**

PCB impedance simulation Approach:

Result = **Parameters** + **Calculator**

$$y = f(x)$$

Parameters

- T [Measurable]
- W/S [Measurable]
- H [Measurable]
- **Dk [Measurable?]**

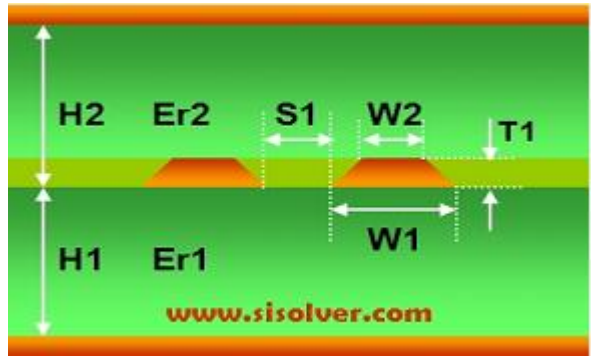
Calculator

Impedance Model

- The key parameters: H, W/S, T can be directly measured, but Dk is an exception

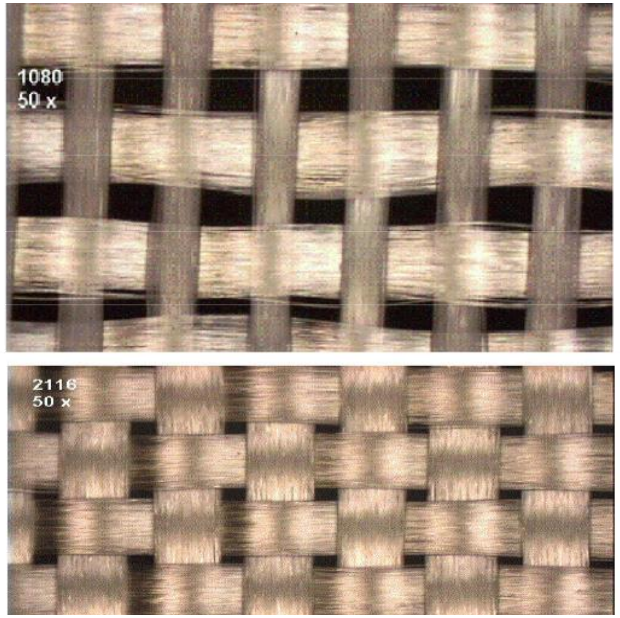
Inaccurate Simulation may comes from:

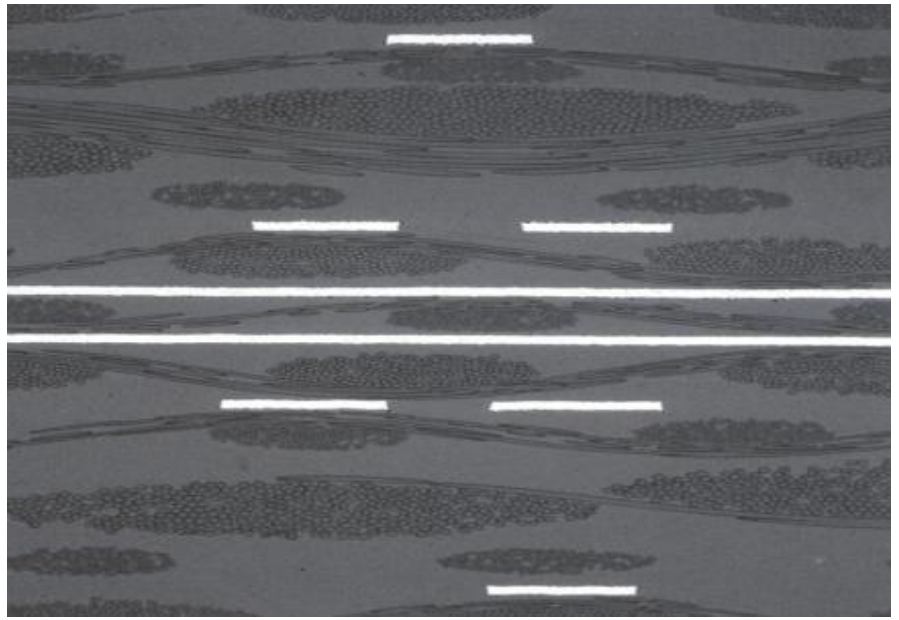
1. **Dk**
2. **Impedance Model**

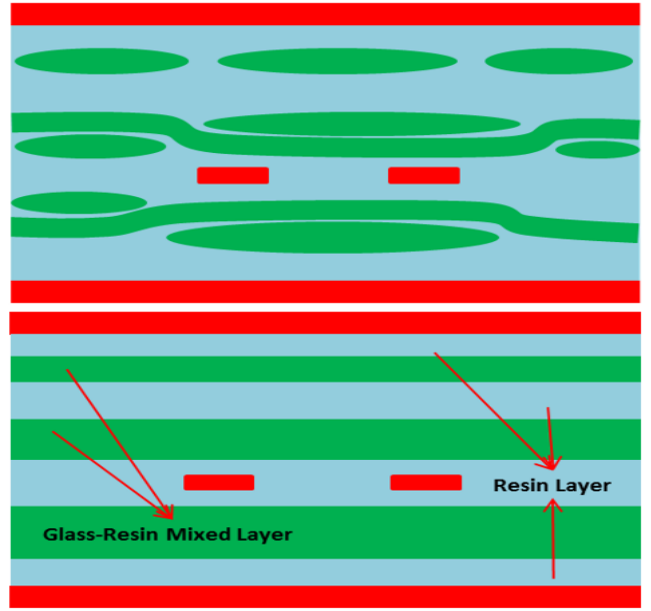


Dk of the PCB FR4 Dielectric:

- PCB FR4 is a mixture dielectric with glass fiber(DK:4.0~6.5) and resin (DK:2.0 ~ 3.5). DK distribution is Non-uniform.
- A single ply of the FR4 material—Prepreg is a variable with different Fiber style and Resin Content.

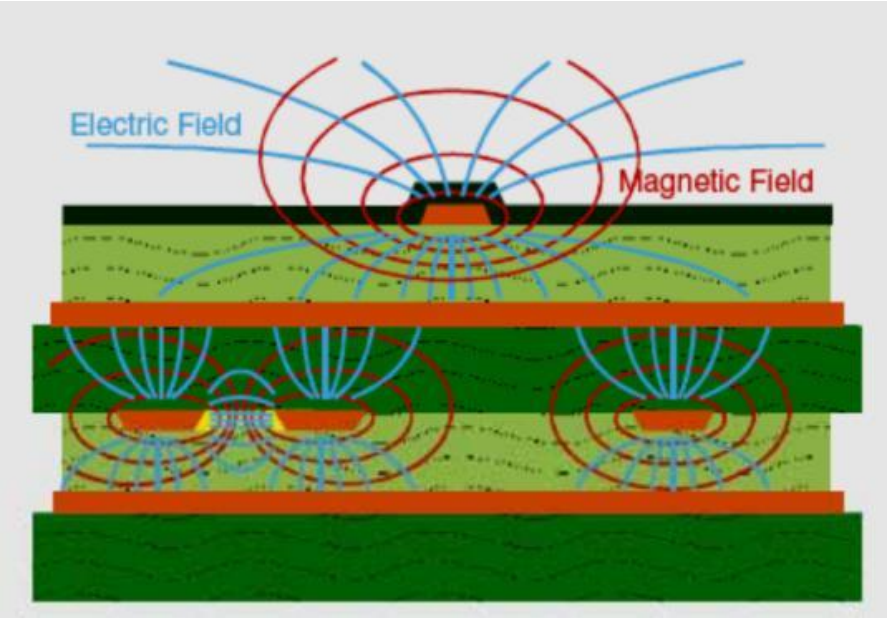


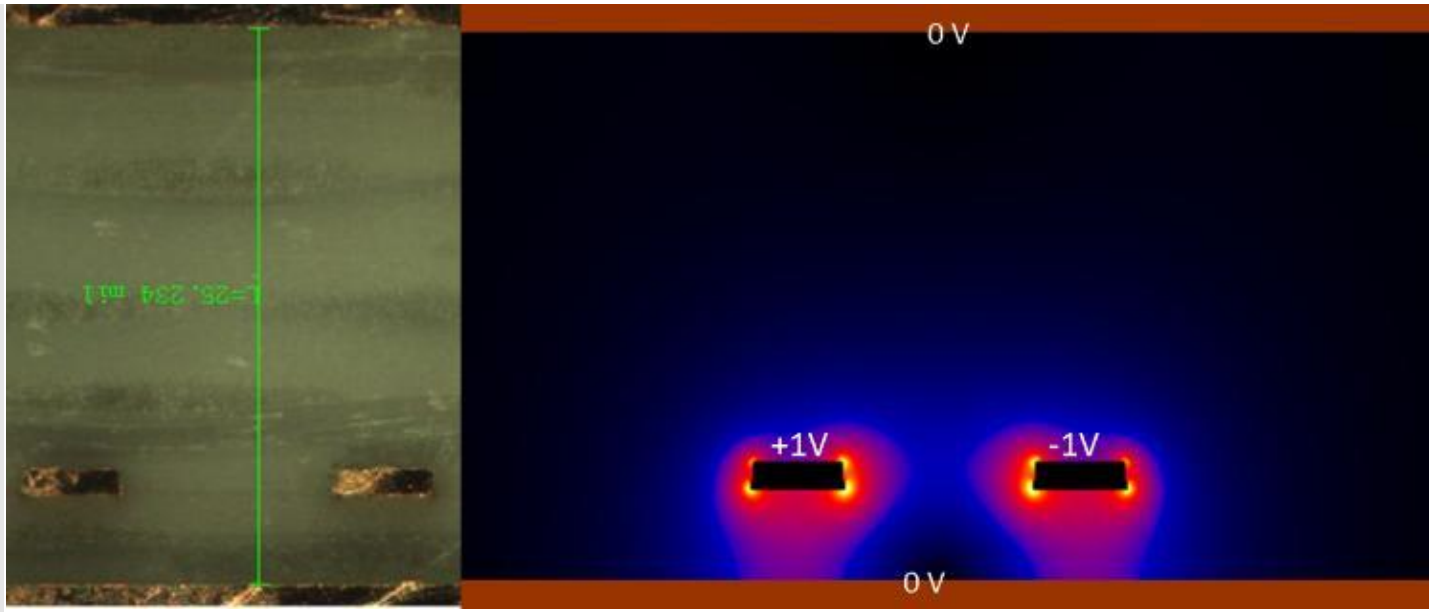




Impedance Model:

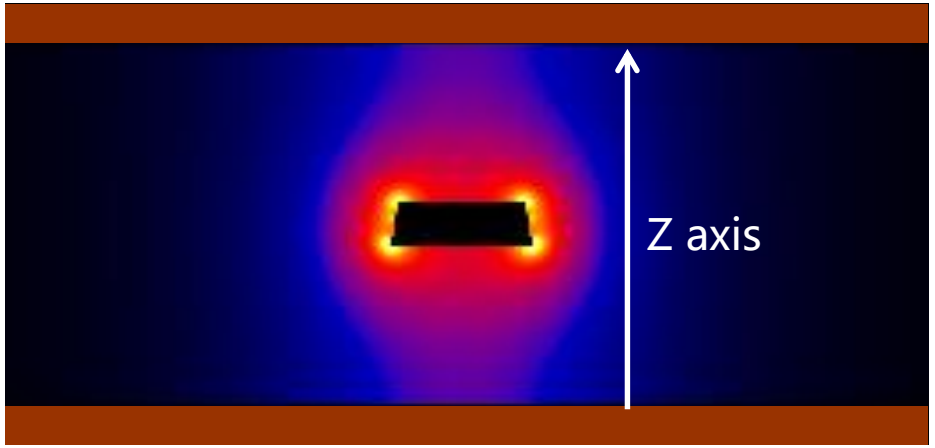
The nature of the impedance model is described by the electromagnetic field distribution

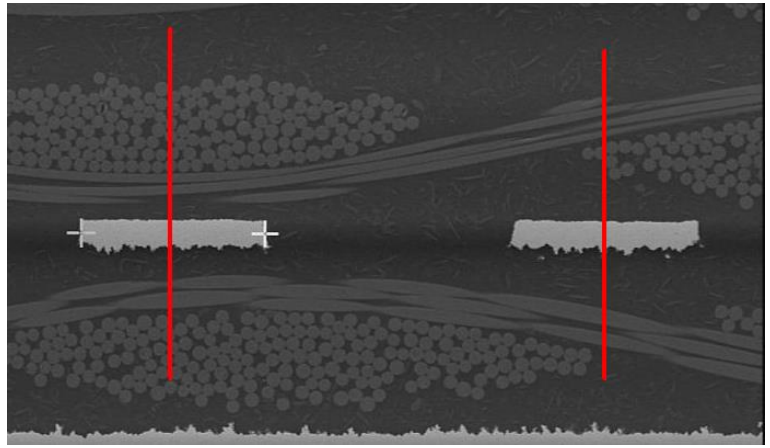




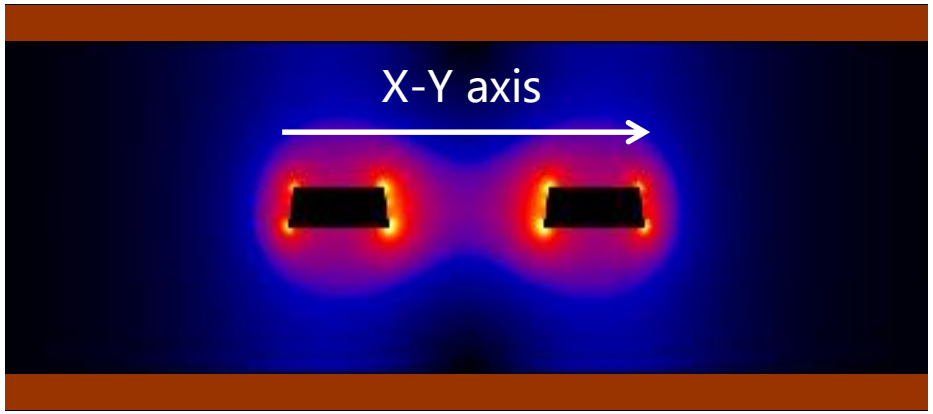
- **The density of the electromagnetic field distribution is Non-uniform**

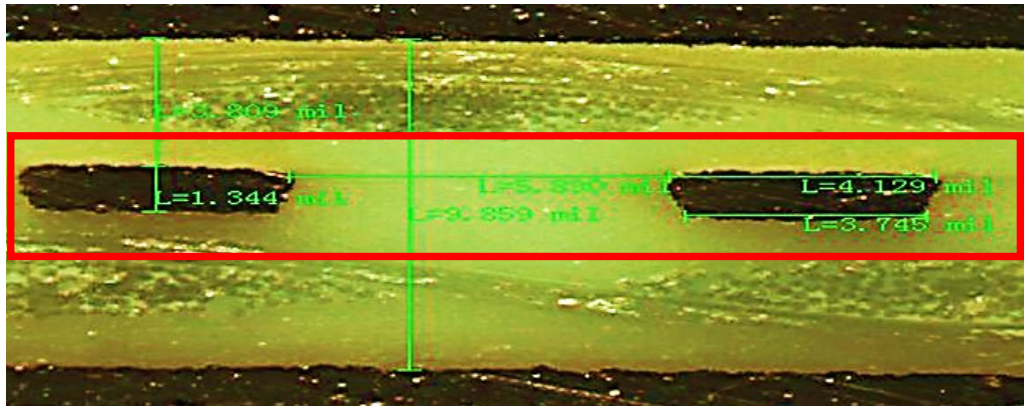
Single-end Model vs. Differential Model:





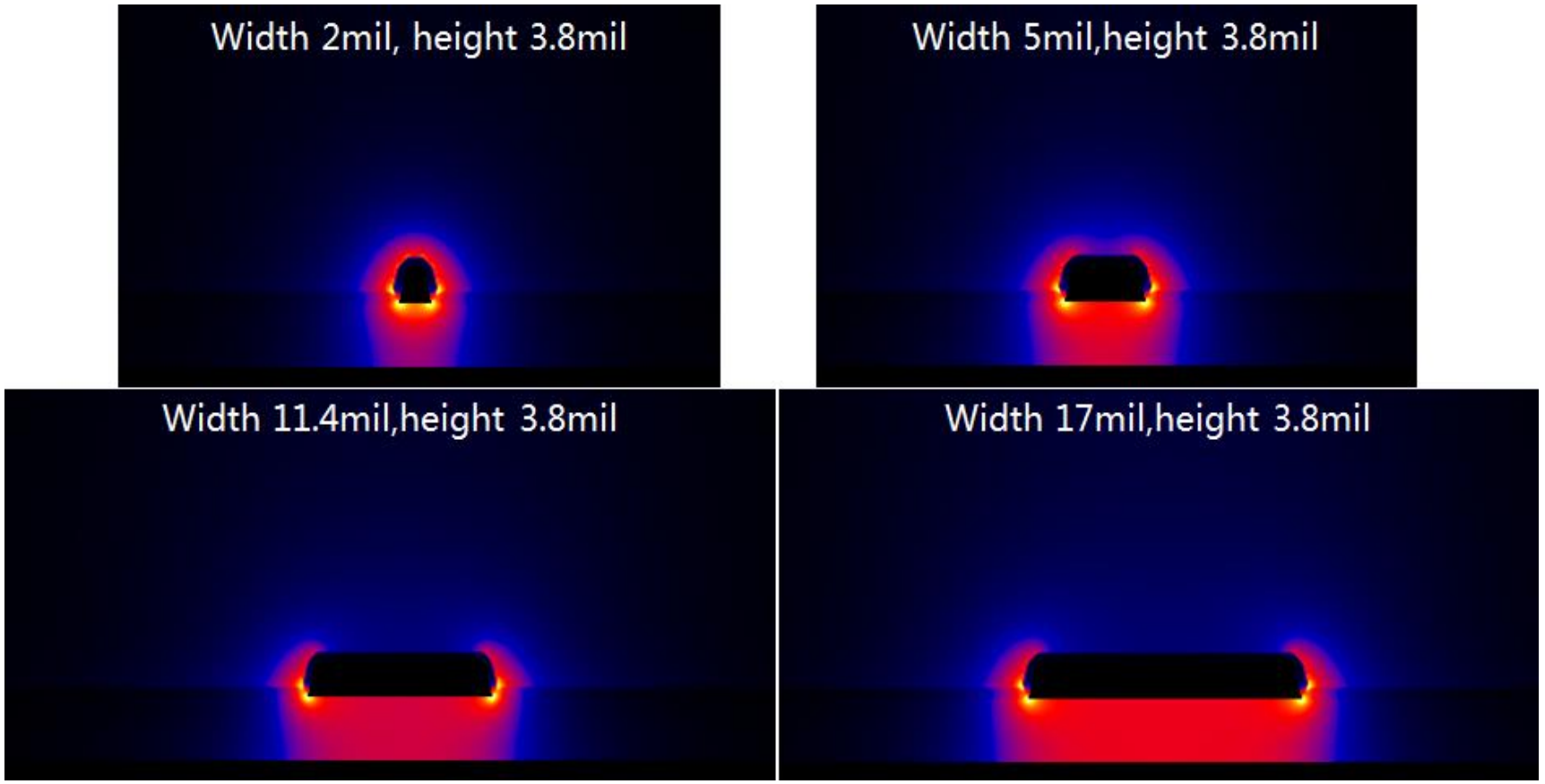
- **Single-end Model is sensitive to the DK on Z axis. And the Dk on Z axis is strongly effected by Fiber Wave Effect.**





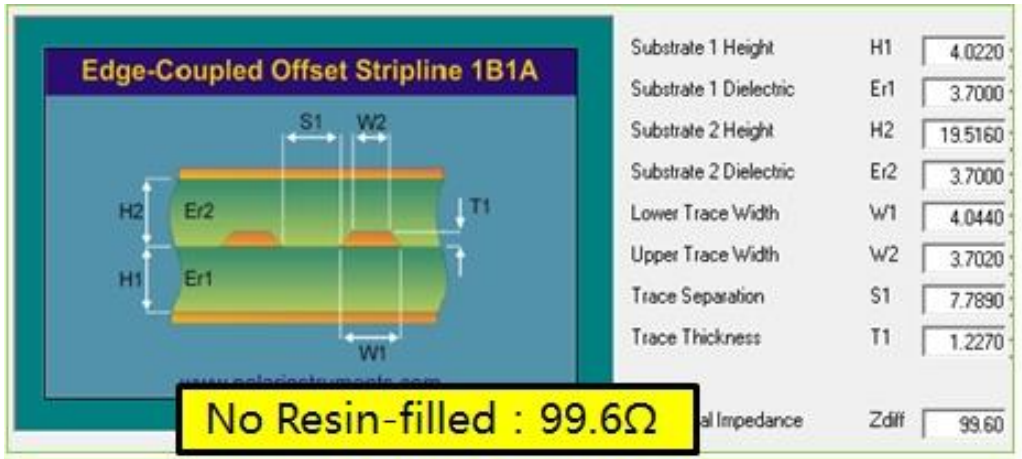
- **Differential Model is sensitive to the DK on X-Y axis. And Pure resin covers the signals on the X-Y axis.**

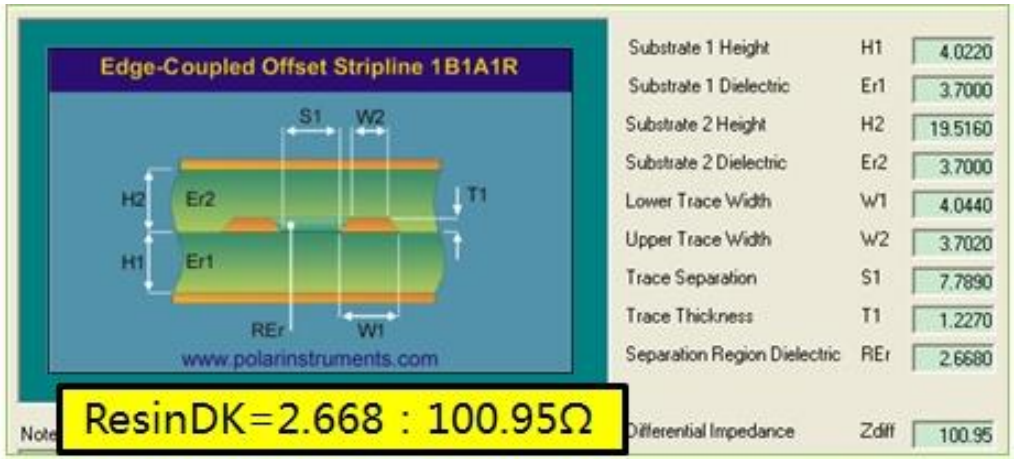
The effect of model geometries:

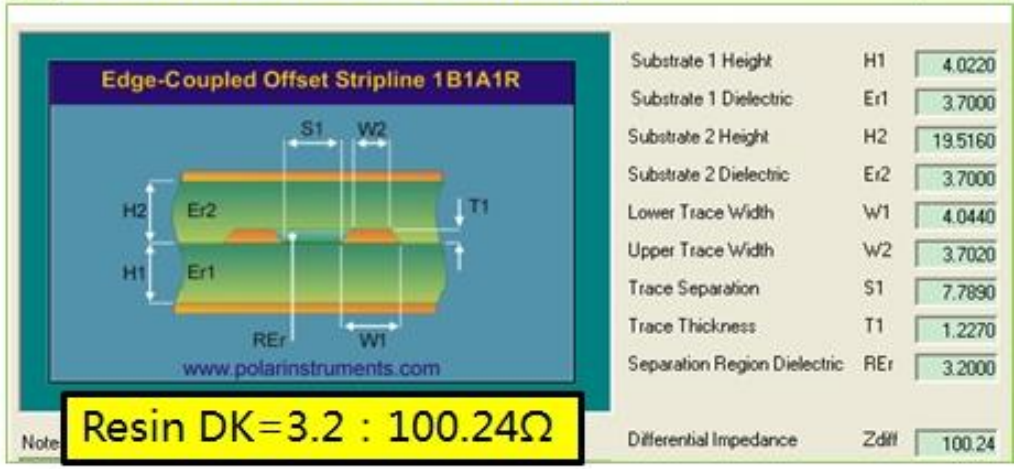


- **the impedance Electromagnetic field distribution will be effected by the model geometries (W,T,H). So on a fixed stack-up (DK distribution is fixed) if the trace width is changed, the final effective DK will be different.**

Impedance Calculator:



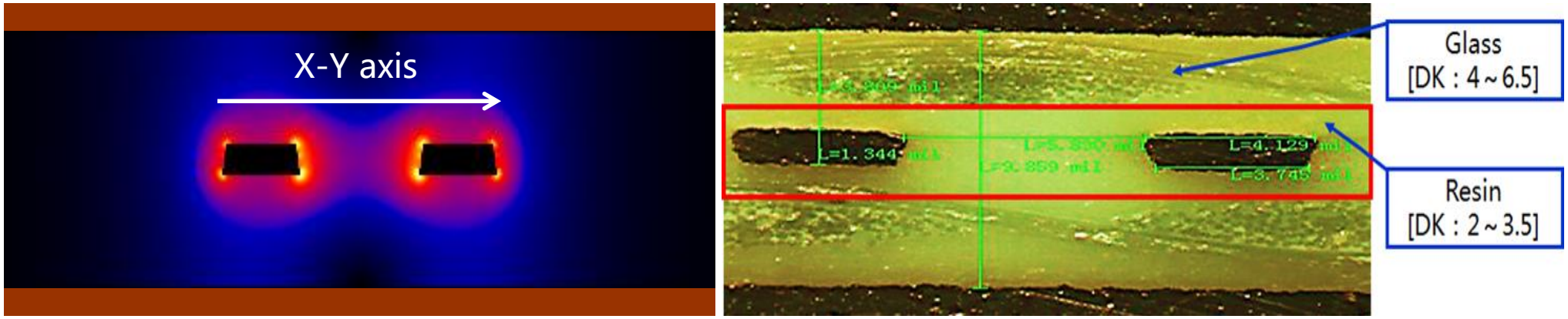




- **Traditional impedance calculator is hard to deal with the FR4 Glass-Resin mixed dielectric**

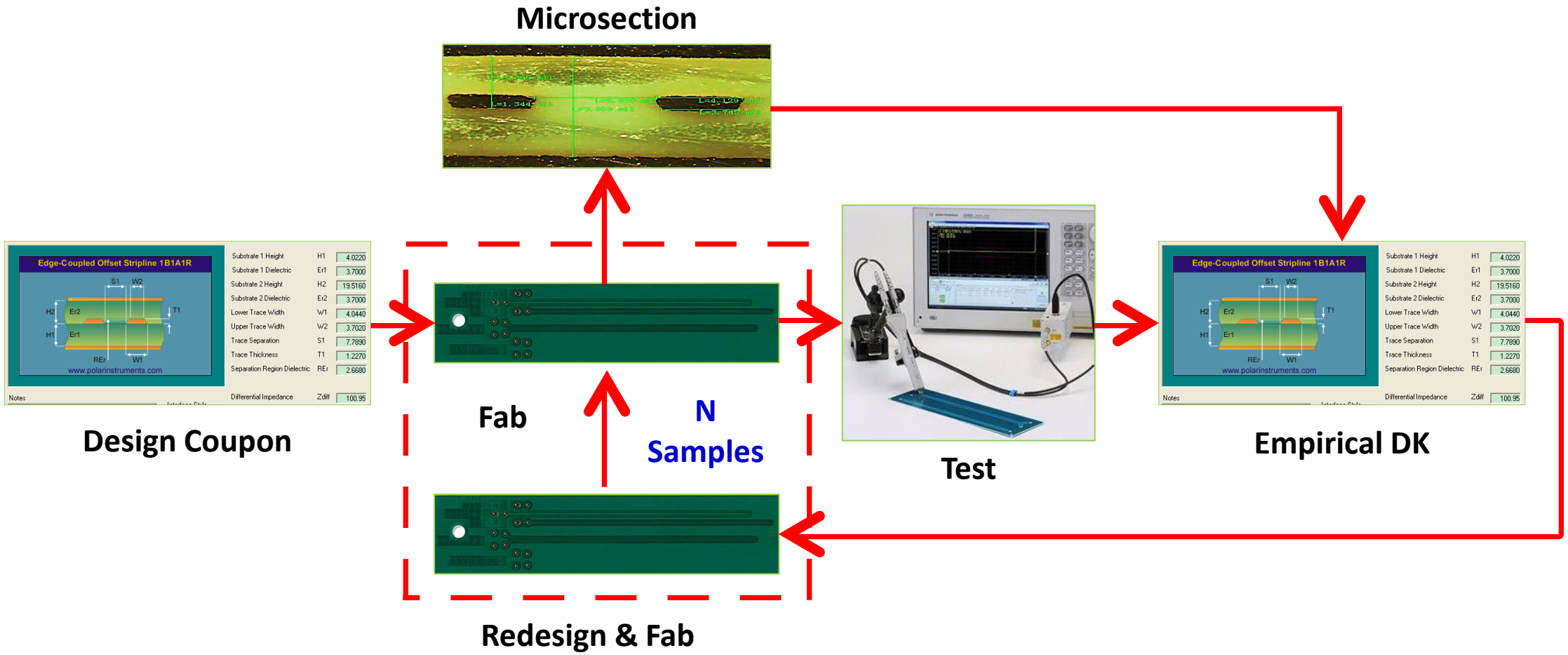
Root Causes of inaccurate Simulation:

- FR4 is a mixture dielectric, Dk distribution is non-uniform.
- Impedance Electromagnetic field distribution is non-uniform



The real effective Dk is multivariable, but we use a fixed Dk for design

Empirical Dk Method:



- Using the Microsection data to back-calculate the Dk is mostly used to meet the target by Fabs

Empirical Dk (database):

Test boards DK analysis Summary					
Base Material	PP Style	DK Simulation			
		CITS25	SI8000	Datasheet	Difference
Isola-FR408	1080 RC63%	3.08	3.12	3.51	0.39
Isola-FR408	2116 RC53%	3.12	3.13	3.73	0.6
Isola-IS415	1080 RC65%	3.05	3.02	3.52	0.5
Isola-IS415	2116 RC55%	3.06	3.08	3.72	0.64
TUC-TU862	1080 RC67%	3.4	3.43	4.1	0.67
TUC-TU862	2116 RC56%	3.63	3.6	4.3	0.7
TUC-TU862	2116 RC60%	3.8	3.81	4.3	0.49
EMC-EM370D	1080 RC63%	3.24	3.28	3.8	0.52
EMC-EM370D	2116 RC52%	3.47	3.44	4.1	0.66
EMC-EM370D	7629 RC44%	3.66	3.7	4.2	0.5
ITEQ-IT200LK	1080 RC65%	3.14	3.15	3.68	0.53
ITEQ-IT200LK	2116 RC57%	3.14	3.13	3.83	0.7
ITEQ-IT200LK	7628 RC50%	3.31	3.3	3.99	0.69

Base on the experiment:

(1) Big off between back-calculated Dk and datasheet .

(2) The same stackup, different impedance model result different back-calculated Dk.

(3) Empirical Dk the average value of N back-calculated DK values.

Conclusion:

Empirical Dk is still a Fixed Value, but real effective Dk is a variable

Drawbacks of the Empirical Dk Method:

- **10% tolerance control capability limit**
- **Black-Box--- nontransparent Impedance design rule**

  the front-end designers (Vendor) use the datasheet Dk, but the Fabs use private empirical Dk
- **Cost and Yield Rate**

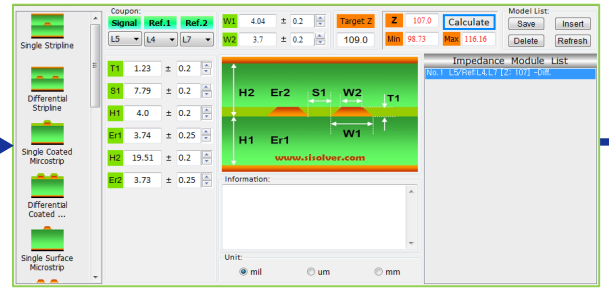
  it's very expensive to build the empirical DK database. The yield rate of the empirical DK method is not as good as expected. the FPY is around 50% ~65%, and even <30% for some NPIs.

Full-factors Cost-effective Method:

DK Measure

DK Database

Stack-up Simulation



Impedance Simulation

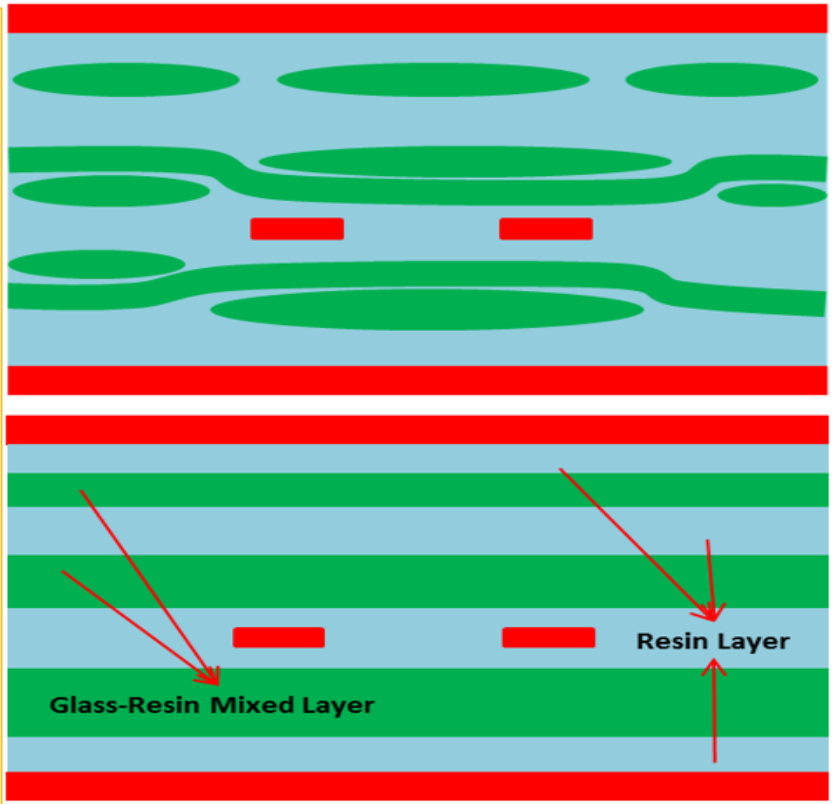
Fab

Key Procedure-----Stack-up Dk Simulation:

1. Dielectric structure stratification
2. Calculating the thickness of each resin layer and glass-resin mixed layer
3. DK simulation(Dk_Resin , Dk_Mixed)

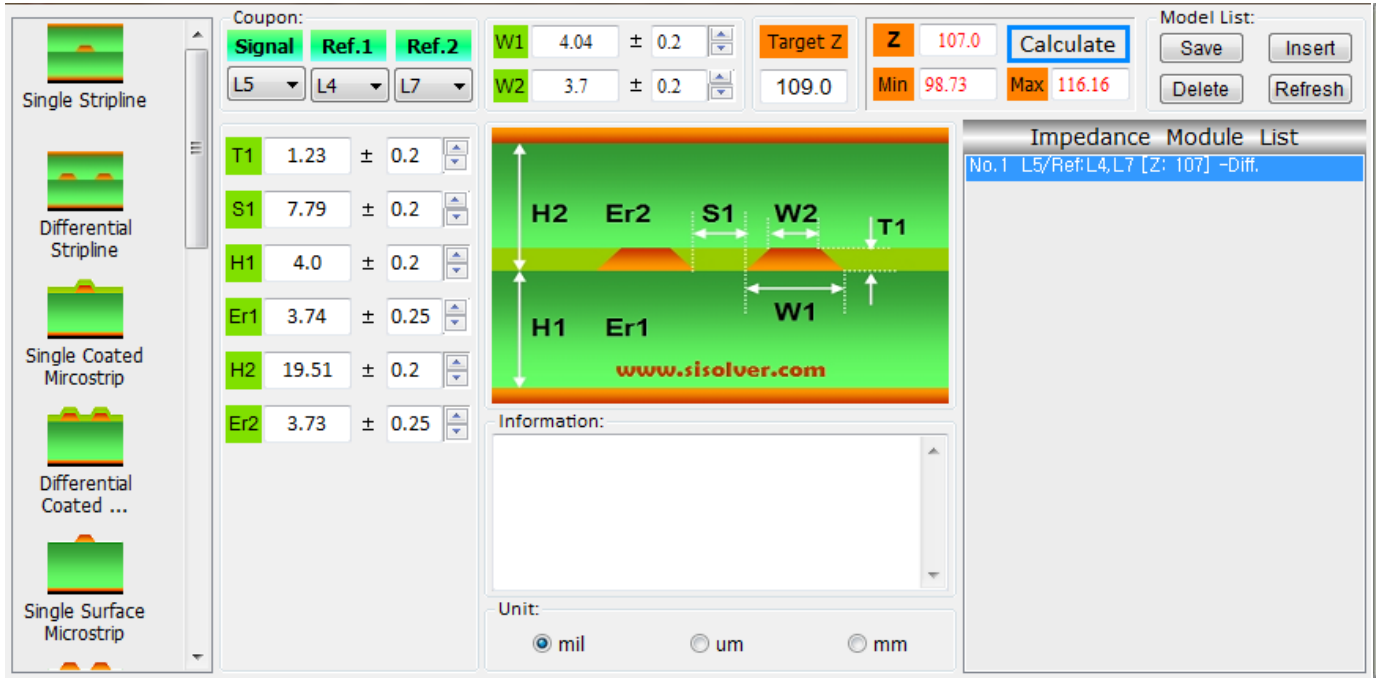
PN:	Layer	Cu_oz	Cu%	PP	RC	THK mil	DK	M_DK	Space mil	BCoat mil
	L1	0.5oz	100%							
				1080	65%	3.1	3.43	3.49	2.87	0.37
	L2	1/1oz	81%			4	3.74	3.74	4	0.45
	L3		75%							
				2116	55%	4.91	3.69	3.81	4.38	0.34
	L4	1/1oz	81%			4	3.74	3.74	4	0.45
	L5		75%							
				2116	55%	4.91	3.69			
				2116	55%	4.91	3.69	3.76	13.83	0.55
				2116	55%	4.91	3.69			
	L6	1/1oz	75%			4	3.74	3.74	4	0.45
	L7		81%							
				2116	55%	4.91	3.69	3.81	4.38	0.34
	L8	1/1oz	75%			4	3.74	3.74	4	0.45
	L9		81%							
				1080	65%	3.1	3.43	3.49	2.87	0.37
	L10	0.5oz	100%							

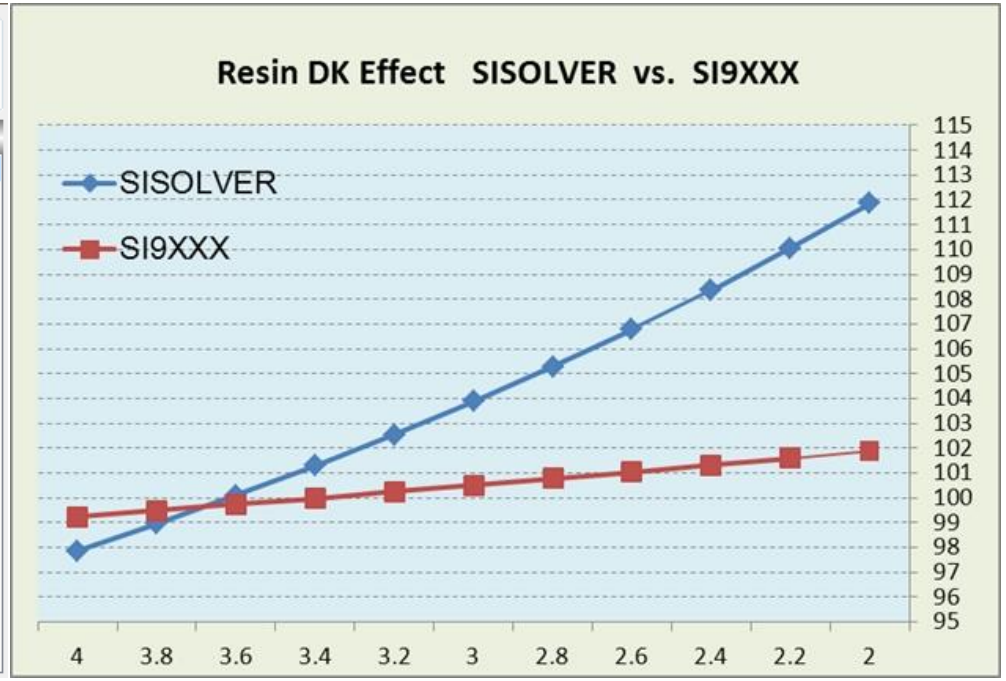
Material: IS415; Thickness: 57.53mil [Nominal]



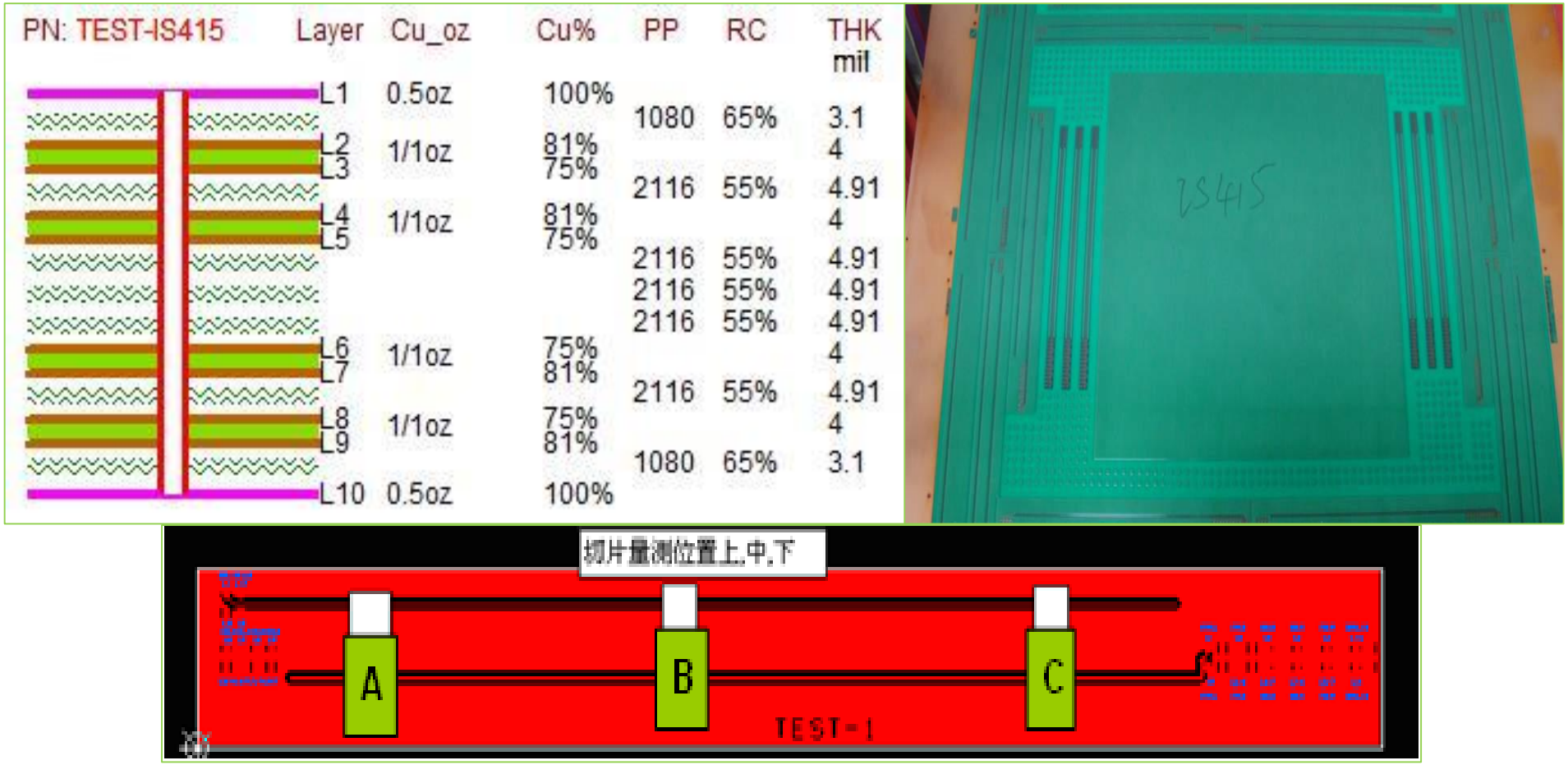
Key Procedure-----Resin-filled layer Impedance Model:

1. Auto-link the Stack-up for Complicated dielectric Parameters
2. Accurate multilayers model field solver with resin-filled layer

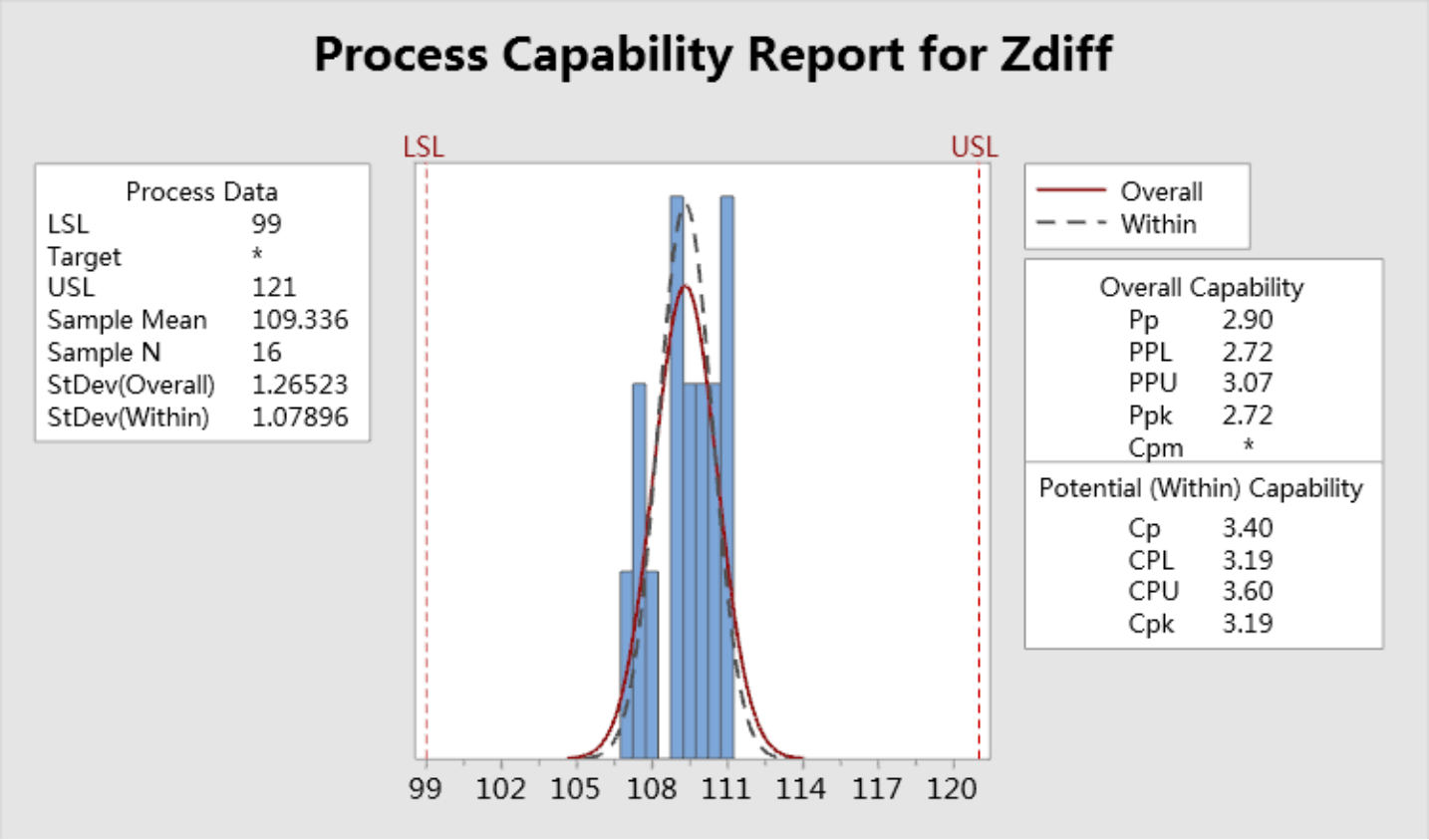




Case Study----Stack-up:



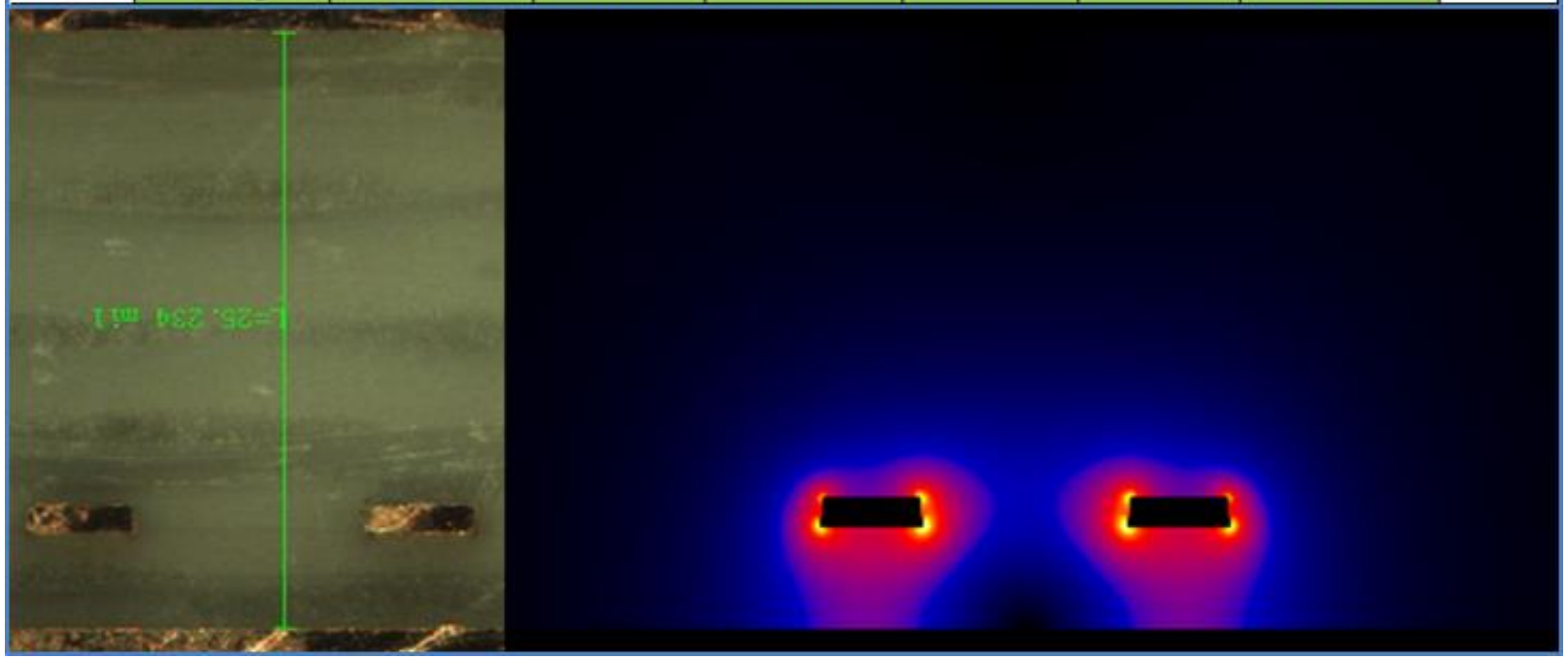
Case Study----Impedance Results:



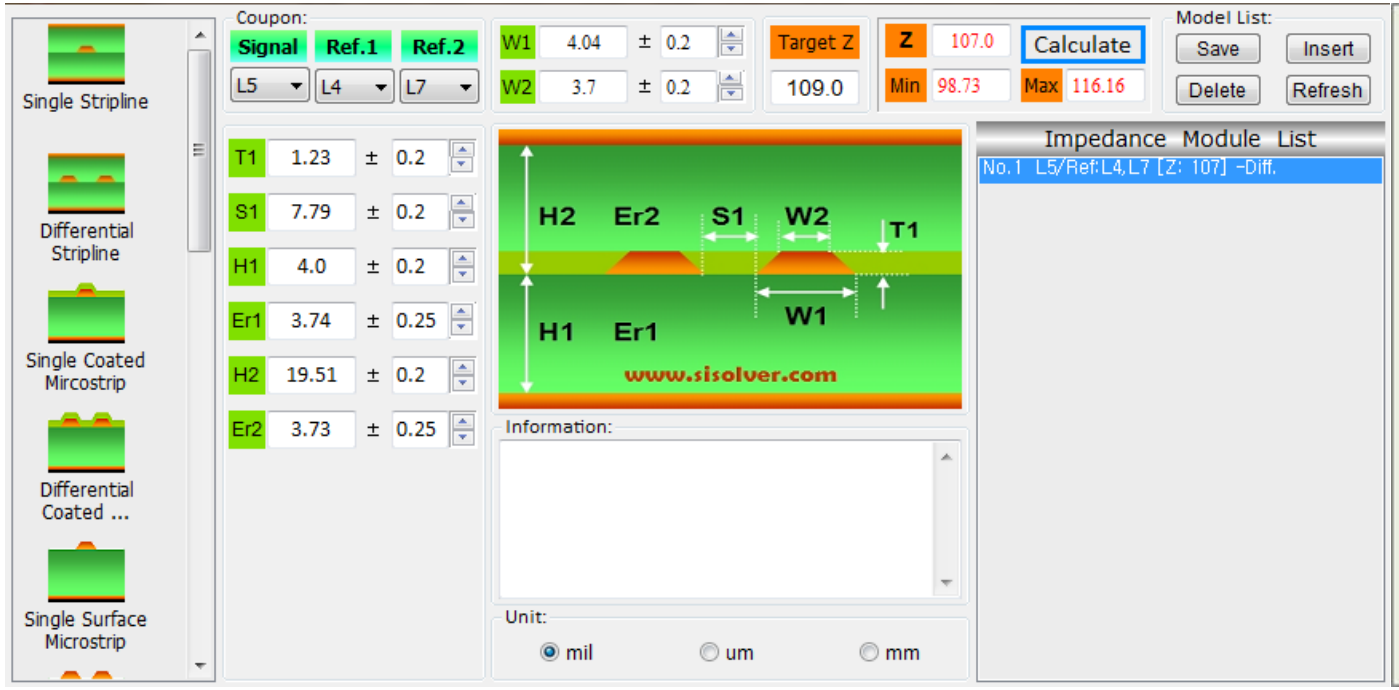
- **Tested 16 coupons, the Cpk is perfect. The manufacturing process is in good control.**

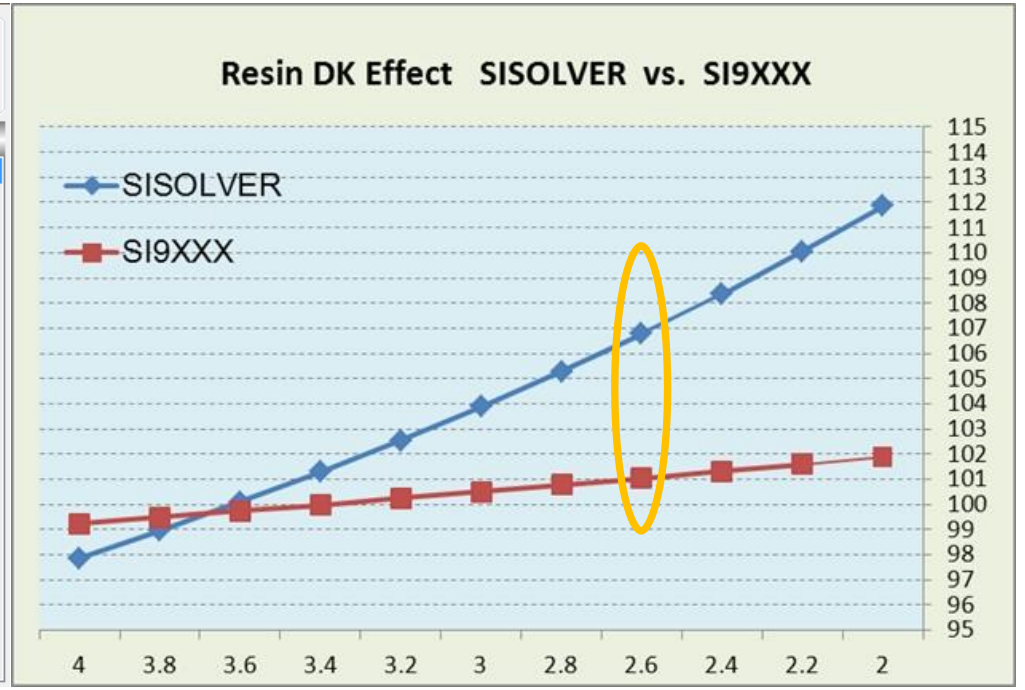
Case Study----Microsection:

Coupon No.	Microsection [Sig:L5; Ref:L4/L7] (mil)							Zdiff (Ohm)
	Location	H(H1+H2)	H1	W2	W1	S	T	
15	A	23.451	4.001	3.777	4.033	7.746	1.152	109.044
	B	24.045	4.129	3.585	4.033	7.842	1.248	
	C	23.120	3.937	3.745	4.065	7.778	1.280	
	Average	23.539	4.022	3.702	4.044	7.789	1.227	



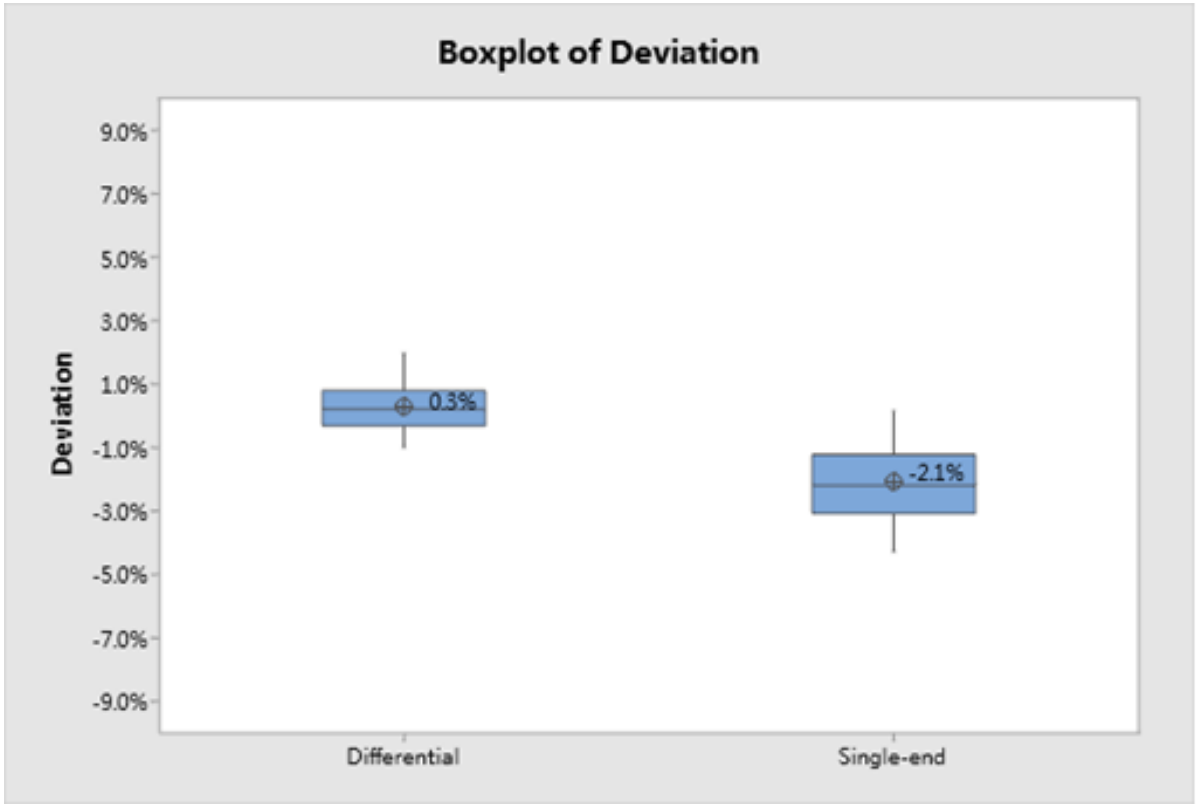
Case Study----Microsection Simulation:

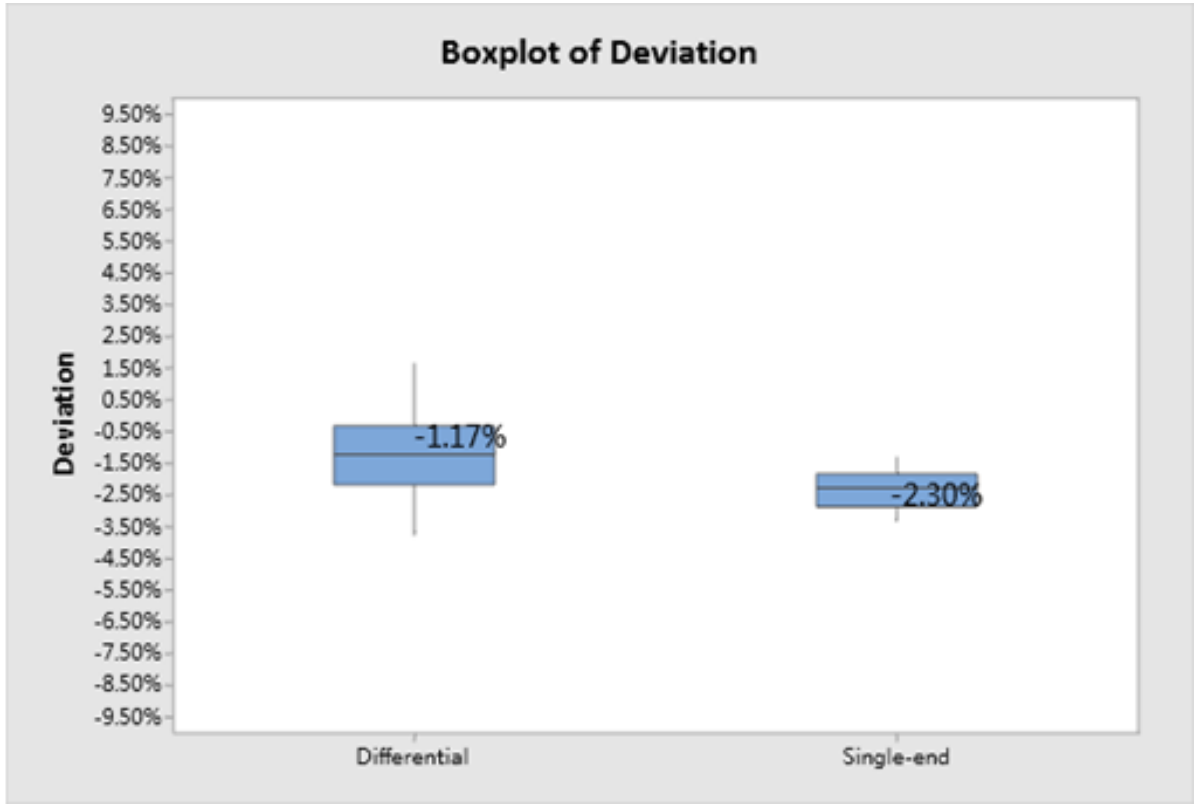




- **The new method is 107 Ohm, closed to the measured 109 Ohm, off by 1.8%.**
- **The traditional field solver is near 100 Ohm, off by 9%.**

Accuracy of the new method:





- The Accuracy of new method is <2.5%(using Microsection to simulate)
- The Single-end model has more variation than the Differential model due to the Fiber Wave Effect

Summary:

- DK of FR4 dielectric and impedance Electromagnetic field is not uniform distribution.
- Traditional method uses a fixed Dk to design, but the real effective DK is multivariable.
- 10% impedance tolerance is the ultimate limit of the empirical DK method.
- Empirical DK method results in the Black-Box of design process and issues on quality, cost and lead-time.
- The introduced new method using the specific stack-up & DK simulation technique and multilayers dielectric field solver with resin-filled layer can achieve <2.5% tolerance.
- The new method is novel and cost-effective without any empirical data involved. It helps to achieve 5% tolerance spec and save lots of cost and time.

Q & A

Thank You！